IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 10/201,208, filed July 22, 2002, ~~pending.~~ now U.S. Patent 6,984,545, issued January 10, 2006.

Please amend paragraph **[0016]** as follows:

[0016] The nature of the present ~~invention~~ invention, as well as exemplary embodiments and other features and advantages of the present ~~invention~~ invention, may be more clearly understood by reference to the following detailed description of the invention, to the appended claims, and to the several drawings herein, wherein:

Please amend paragraph **[0022]** as follows:

[0022] It will be appreciated that the drawings described herein are not drawn to scale, but are for exemplary purposes only. Referring now to drawing FIG. 1A, there is shown a cross-sectional view of an assembly generally at 10 that includes a solder mask 12 according to the present invention and a carrier substrate 15 upon which the solder mask 12 is carried. In the illustrated embodiment, the carrier substrate 15 is an interposer with opposite major upper and lower surfaces 16 and 18, respectively. A slot 17 or other opening is formed through the carrier substrate 15, somewhat centrally in the depicted embodiment, and extends from upper surface 16 to lower surface 18. As known to those of ordinary skill in the art, the carrier substrate 15 may be formed to a desired shape and thickness and with required features for use in forming a functional semiconductor package.

Please amend paragraph **[0023]** as follows:

[0023] The material used to fabricate the carrier substrate 15 may comprise a relatively thin, flexible film of an electrically insulative material, such as an organic polymer resin (e.g., polyimide). If the carrier substrate 15 comprises an MTBGA substrate, the thickness ~~othereof~~ thereof may be on the order of about 50 μm to about 75 μm. Alternatively, the carrier

substrate 15 may comprise a somewhat rigid, substantially planar member, which may be fabricated from any known, suitable materials, including, but not limited to, insulator-coated silicon, a glass, a ceramic, an epoxy resin (e.g., FR-4, FR-5, etc.), bismaleimide-triazine (BT) resin, or any other material known in the art to be suitable for use as a carrier substrate. A BT resin substrate may have a thickness of about 125 μm. Although the illustrated embodiment depicts the carrier substrate 15 as being an interposer, a solder mask 12 incorporating teachings of the present invention may also be used with other types of carrier substrates, such as circuit boards, leads, and the like, without departing from the scope of the present invention.

Please amend paragraph **[0024]** as follows:

[0024] As shown, the upper surface 16 of the carrier substrate 15 carries conductive traces 19, first contact areas 21 located proximate the slot 17, and second contact areas 22 located peripherally relative to the first contact areas 21. As shown, the second contact areas 22 are arranged in an area array, although other arrangements of second contact ~~areas~~ <u>areas 22</u> are also within the scope of the present invention. It will be appreciated that the conductive traces 19, first contact areas 21, and second contact areas 22 may comprise, without limitation, conductively doped polysilicon, a conductive metal or metal alloy, conductive or conductor-filled elastomer, or any other conductive material used for electrical connections known to those of ordinary skill in the art.

Please amend paragraph **[0027]** as follows:

[0027] As an example of fabrication of the solder mask, known photolithography processes may be employed. When ~~photolithograpy~~ <u>photolithography</u> processes are used, a layer of dielectric photoimageable material, such as a photoresist, may be formed on the upper surface 16 of the carrier substrate 15 by known processes, such as by spin-on techniques. The photoimageable material may then be selectively exposed or patterned, then developed, followed by removal of unpolymerized portions thereof to form the solder mask 12 therefrom.

Please amend paragraph **[0029]** as follows:

[0029] In yet another exemplary method, a solder mask 12 may be formed as either a single layer ~~or a~~ or as a plurality of contiguous, at least partially superimposed, mutually adhered layers of dielectric material by known stereolithography techniques. In such techniques, selected regions of a layer of at least partially unconsolidated material, such as an uncured photoimageable polymer, are selectively consolidated, such as by exposing the uncured photoimageable polymer in the selected regions to an energy beam comprising a curing wavelength of radiation. This process may be repeated until a structure of the desired height is formed.

Please amend paragraph **[0037]** as follows:

[0037] Referring now to FIG. 3, there is shown an inverted perspective view of a semiconductor device assembly 10′ that includes ~~openings~~ a slot 17′ and an opening 38′ in the carrier substrate 15′ and the adhesive element 32′, respectively, that extend beyond at least one outer peripheral edge of the semiconductor die 24, leaving a space 44 uncovered by the semiconductor die 24. A coverlet 47, such as a film, tape, or other substantially planar member, is secured to the upper surface 20 (now inverted) of the solder mask 12. The coverlet 47 may be at least partially coated with an adhesive material 50 to secure the same to the upper surface 20 of the solder mask 12. The adhesive material 50 used on the coverlet 47 facilitates the ready removal of the coverlet 47 from the upper surface 20 of the solder mask 12. The coverlet 47 may also have sufficient flexibility to conform to any irregularities or ~~nonplanaraties~~ nonplanarities of the upper surface 20 of the solder mask 12.

Please amend paragraph **[0038]** as follows:

[0038] An encapsulant material 46 (FIG. 4) may be introduced into the bottom side 36 of the assembly 10′ through the space 44, which is continuous with the slot 17′ of the carrier substrate 15′ and the central opening 13 of the solder mask 12, by way of an encapsulant dispenser needle 48 or otherwise, as known in the art. The coverlet 47 precludes loss of

encapsulant material 46 during inversion of assembly 10′. Air may be displaced by encapsulant material 46 through the open space 44 at the end of the slot 17′, opposite that into which the encapsulant material 46 is introduced.

Please amend paragraph **[0040]** as follows:

[0040] Solder balls or other discrete conductive elements 52 (FIG. 1B) may then be formed by known processes, such as by immersing ~~the assembly~~ assembly 10 in a solder bath.